REMARKS

Claims 9-11, 18, 19 and 23 have been canceled. Claims 1-8, 12-17, 20-22 and 24-30 are now pending in this application. Reconsideration of the application is earnestly requested.

The Office action summary does not indicate whether the drawings filed have been accepted or objected to by the Examiner. The drawings are formal in nature and Applicant requests that the next communication indicate whether or not these drawings have been accepted.

The Office action has rejected claims 1-11, and 13-29 under 35 U.S.C. 103 as being unpatentable over Intel (IA-32® Architecture Software Developer's Manual, Volumes 1-2, 2002; "*Intel*") and *Killian et al.* (U.S. Patent No. 5,420,992), "*Killian.*" Although the Examiner's arguments have been carefully considered, Applicant respectfully traverses these rejections as explained below.

The claims have been amended to make clear that common subcircuitry is used to perform sign extensions not only on an immediate field of a non-branch instruction, but also to perform sign extensions on the same immediate field of branch instructions. Figure 4 illustrates an immediate field 405 of a branch instruction and Figure 5 illustrates the same immediate field 505 of a non-branch instruction. The advantage is pointed out in the specification:

"Because both branch and non-branch operations perform a sign extended operation on the immediate field value, the same subcircuit can be reused for both types of operations. Using the same subcircuitry allows efficient use of hardware resources and reduced processor core sizes." (Page 12, lines 24-27.)

Claim 1

The limitations of claims 9-11 have been incorporated into claim 1 in order to make clear that common subcircuitry is used to perform sign extensions not only on an immediate field of a non-branch instruction, but also to perform sign extensions on the same immediate field in branch instructions. Claim 1 specifically requires:

common subcircuitry operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate field in branch instructions to calculate a target address for branch instructions.

Thus, the same subcircuitry can be used for branch and non-branch instructions to perform a sign extension of a value in the immediate field.

By contrast, the cited art of record does not teach this element of claim 1. The Office action agrees that *Intel* does not teach this element and relies upon *Killian*, specifically, column 8. Column 8 does disclose that in the case of load and store instructions, the immediate field is sign extended, and that also in the case of branch instructions the immediate field is also sign extended (lines 1-13). But, there is no common subcircuitry disclosed that his operable to perform both sign extensions of immediate fields in non-branch instructions as well as a sign extensions of immediate fields in branch instructions.

The Examiner's attention is drawn to Figure 3C and the accompanying disclosure at column 11. This figure shows quite clearly at the top right that subcircuitry 85 (and its inputs) is used to calculate a branch target address which includes performing a sign extension of a 16-bit immediate field in the branch instruction. This subcircuitry is entirely separate from circuitry at the top left of the figure. Circuitry at the top left includes an adder 77, a base address, and a sign extension circuit 78 for the purposes of computing load and store instructions. Thus, circuitry at the top left for performing a sign extension of an immediate field for a non-branch instruction is entirely separate from circuitry at the top right for performing a sign extension of an immediate field in a branch instruction. The two different circuits are not common. Claim 1 specifically requires common subcircuitry that operates upon an immediate field for both non-branch and branch instructions. *Killian* teaches away from the present invention by requiring two different circuits for two different types of instructions thus requiring more space and more hardware. For this reason, it is requested that the rejection of claim 1 be withdrawn.

Since dependent claims 2-8, 12 and 13 depend from the independent claim 1, it is respectfully submitted that they are each patentable over the art of record for at least the same reasons as set forth above with respect to the independent claim 1.

Claim 14

The limitations of claims 18 and 19 have been incorporated into claim 14 in order to make clear that common subcircuitry is used to handle a sign extension of both an immediate field of a non-branch instruction as well as an immediate field of a branch instruction. Claim 14 specifically requires:

> common subcircuitry that performs a sign extension of an immediate field associated with one or more branch instructions and that performs a sign extension of said immediate field associated with one or more non-branch instructions.

By contrast, *Killian* does not teach this element of claim 14 as discussed above. For this reason, it is requested that the rejection of claim 14 be withdrawn.

Since dependent claims 15-17 depend from the independent claim 14, it is respectfully submitted that they are each patentable over the art of record for at least the same reasons as set forth above with respect to the independent claim 14.

Claims 20 and 27

The limitation of claim 23 has been incorporated into claim 20 in order to make clear that common subcircuitry is used to handle a sign extension of both an immediate field of a non-branch instruction as well as an immediate field of a branch instruction. Claim 20 specifically requires:

> calculating a branch target address by determining a sign extended value of the immediate value, wherein the branch target address is determined by using common subcircuitry, the common subcircuitry operable to calculate a byte-aligned address, wherein the common subcircuitry is also operable to determine a sign extended value of said immediate field of non-branch instructions.

By contrast, *Killian* does not teach this element of claim 20 as discussed above. For this reason, it is requested that the rejection of claim 20 be withdrawn.

Since dependent claims 21, 22 and 24-26 depend from the independent claim 20, it is respectfully submitted that they are each patentable over the art of record for at least the same reasons as set forth above with respect to the independent claim 20.

Claim 27 includes the same limitations as claim 20 and is believed patentable for the same reasons. Since dependent claims 28-30 depend from the independent claim 27, it is

respectfully submitted that they are each patentable over the art of record for at least the same reasons as set forth above with respect to the independent claim 27.

Reconsideration of this application and issuance of a Notice of Allowance at an early date are respectfully requested. If the Examiner believes a telephone conference would in any way expedite prosecution, please do not hesitate to telephone the undersigned at (612) 252-3330.

Respectfully submitted,
BEYER WEAVER LLP

/Jonathan O. Scott/

Jonathan O. Scott
Registration No. 39,364

BEYER WEAVER LLP
P.O. Box 70250
Oakland, CA 94612-0250

Telephone: (612) 252-3330
Facsimile: (612) 825-6304

;